TOFLAR ASIC for LIDAR applications

The PETsys high performance LIDAR ASIC is a new 64 channel chip for the readout and digitization of signals from SiPM photon detectors in LIDAR applications. It uses a combination of discriminators for best timing and background rejection. All thresholds are separately configurable to a value that can be different for each channel. Every time one of the 64 channels exceeds the trigger threshold a record is created giving the channel number, the time and the charge of the event. Activity in one channel does not cause any dead-time in the other channels.

The main features of the PETsys LIDAR ASIC are:

1. Excellent time resolution. The time resolution for Single Photon events (SPTR) is better than 100 ps (rms).

2. Large dynamic range: The ASIC measures SiPM pulses in the range from 1 photon to 10^4 photons (SiPM gain $=10^6$).

3. Noise filtering and baseline stabilization. Noise filtering and baseline stabilization module reduces the SiPM dark noise and eliminates the baseline fluctuations due to pileup of closely spaced events.

4. High data rate. The ASIC accepts events at input rate of 1 M events/s per channel.

5. Short interval between pulses. Pulse filtering allows discrimination of pulses separated by 5 ns (SiPM type dependent).

6. Deep event buffer: The ASIC is able to store the timing and amplitude information of 32 shortly spaced consecutive events.

7. Amplitude measurement. Pulse amplitude measurement is performed in the full input dynamic range using Time Over Threshold and/or Charge to Amplitude Converter.

8. Internal references. Precise voltage and current internal references with minimal dependence on Process, Voltage and Temperature variations.
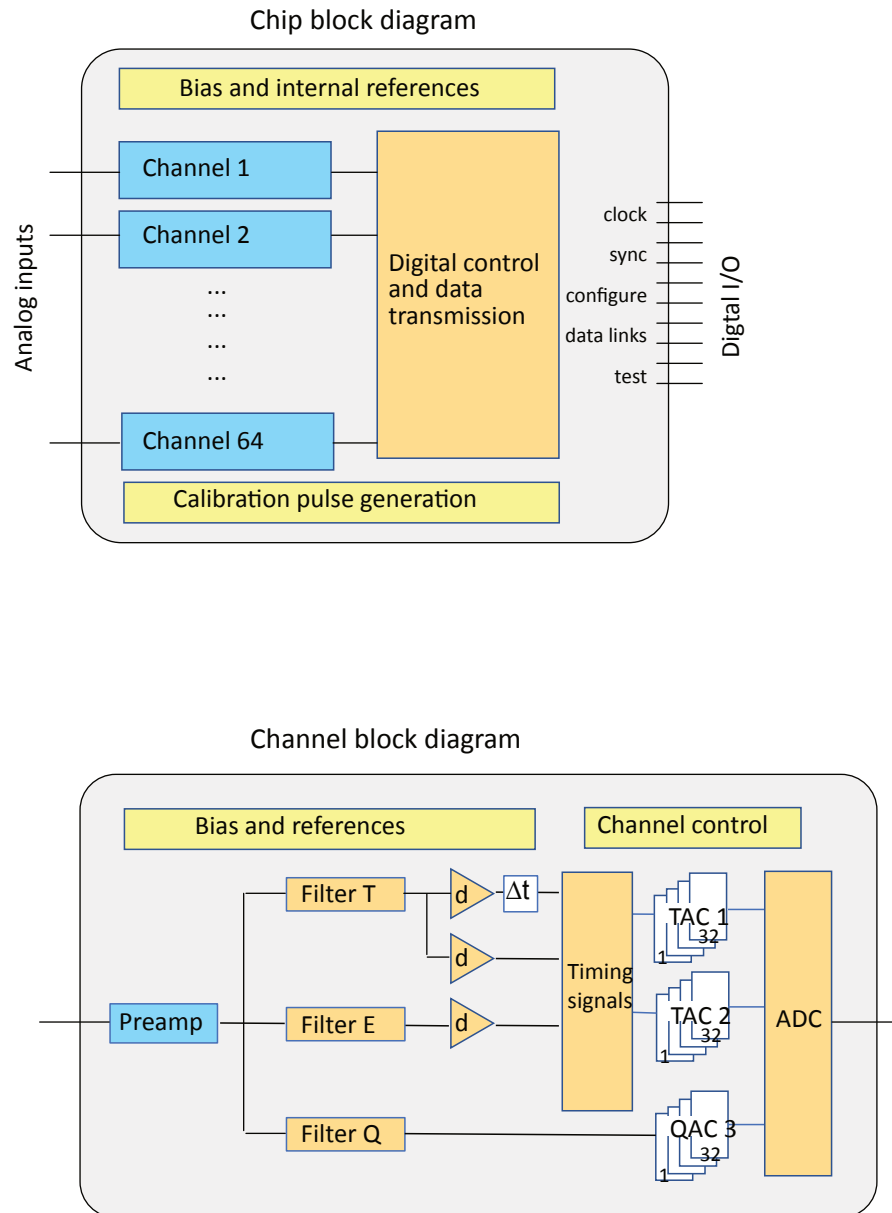
Other features of the PETsys LIDAR ASIC are:

- Input dynamic range: 100 fC to 1 nC.

- Separately configurable timing and trigger thresholds for each channel.

- Time to Amplitude Converters (TAC) for measurement of Time-of-Arrival (ToA) and Time-over-Threshold (ToT) in each channel.

- Charge to Amplitude Converter (QAC) for pulse energy measurement.

- Time and charge digitization with a Successive Approximation (SAR) ADC of 10-bit.

- TDC time binning: 10 ps.

- On-chip calibration pulse generator with programmable amplitude.

- Fully digital output with 4 LVDS data links double data rate (DDR) compatible.

- Max output data rate: 3.2 Gb/s.

- Clock frequency: 200 MHz.

- Power consumption per channel: 10 mW.

Visit our web site www.petsyselectronics.com
or contact   sales@petsyselectronics.com

Figure 1: Simplified block diagram of the TOFLAR ASIC.

Chip block diagram

- Bias and internal references
- Channel 1
- Channel 2
- ...
- Channel 64
- Calibration pulse generation
- Digital control and data transmission
- Analog inputs
- Digtal I/O
  - clock
  - sync
  - configure
  - data links
  - test

Channel block diagram

- Bias and references
- Channel control
- Preamp
- Filter T
- Filter E
- Filter Q
- Δt
- Timing signals
- TAC 1 (1...32)
- TAC 2 (1...32)
- QAC 3 (1...32)
- ADC